

IN THE CLAIMS

Please amend claims 20 and 30, as follows:

20. (AS ONCE AMENDED) The data scrambling method of claim 17, wherein the generating of the random data comprises shift-storing,  $n$  bits in registers and then, generating random data, wherein a total of  $n$  values are used as initial values, including a first initial value, first register values, which are obtained by shifting the first initial value 7 times, a second initial value immediately after a capacity required for return of the first initial value and the first register values, and second register values, which are obtained by shifting the second initial value 7 times,

wherein the data scrambling method further comprises exclusive-ORing outputs of a predetermined number of least significant ones of the registers and input data in units of byte[ ].

30. (AS ONCE AMENDED) The data scrambler of claim 1, wherein the random data generator comprises:

a decoder to selectively output  $n$  bits as valid and invalid bits in response to input  $m$  bits;

$n$  registers arranged in serial, which shift and store the  $n$  bits, to generate shifted  $n$  bits as the random data;

a selection circuit which selects a predetermined value or the shifted  $n$  bits for ones of the shifted  $n$  bits, to generate a selection signal; and

logic gates arranged in serial, which perform XOR operations on the ones of the shifted  $n$  bits, the ones of the shifted  $n$  bits, and an output of an adjacent more significant one of the logic circuits, wherein the output of the logic gate associated with a least significant of the ones of the shifted  $n$  bits is fed back to a least significant one of the registers.